REMARKS

Claim Rejections – 35 U.S.C. §112

Examiner has rejected Claims 1-5 under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention, arguing that the phrase "such that" is similar to "such as" and renders the claim indefinite because it is unclear whether the limitations following the phrase are part of the claimed invention. MPEP §2173.05(d).

Examiner also argues that the limitation "wherein said set of test inputs are applied such that adjacent tracks in said first set of tracks have different logic values and adjacent tracks in said second set of tracks have different logic values" renders the claim indefinite because, as read, the Examiner interprets this language different from what is implied in the specification.

Applicant respectfully submits that the §112 is moot, as the language at issue has been removed from the claims. Therefore, Applicant respectfully submits that Claims 1-5 are currently in condition for allowance. Reconsideration and withdrawal of the rejection is respectfully requested.

Claim Rejections – 35 U.S.C. §103

Claims 1-3 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Abramovici et al. (US 6,108,806), in view of Andrews et al. (US 6,064,225), in further view of Kean (US 6,292,018), in even further view of Das et al. (A Low Cost Approach for Detecting, Locating, and Avoiding Interconnect Fault in FPGA-Based Reconfigurable Systems).

For a §103 obviousness rejection to be proper, the Examiner must meet the burden of establishing that all elements of the invention are disclosed in the prior art; that the prior art relied upon, coupled with knowledge generally available in the art at the time of the invention, must contain some suggestion or incentive that would have motivated the skilled artisan to modify a reference or combined references; and that the proposed modification of the prior art must have had a reasonable expectation of success, determined from the vantage point of the skilled artisan at the time the invention was made. MPEP 2143.

Claim 1 recites a method of testing the routing circuitry in a field programmable gate array (FPGA) having a first FPGA tile, "wherein said first FPGA tile comprises a plurality of interface groups (IGs), each of said IGs having a plurality of input multiplexers configurable to select signals received from outside of said FPGA tile and provide signals to said routing circuitry inside said FPGA tile, and a plurality of input/output pads (I/Os) coupled to at least one of said input multiplexers of at least one of said IGs."

Applicants respectfully submit that the cited prior art fails to disclose an FPGA tile comprising a plurality of interface groups, wherein *each* of the interface groups has a *plurality* of input multiplexers, as recited in Claim 1. On Page 5 of the Office Action dated October 19, 2006, Examiner admits that Abramovici does not teach each of the interface groups having a plurality of input multiplexers. However, Examiner argues that Andrews teaches a conventional FPGA consisting of an array of programmable logic cells 102 surrounded by a ring of programmable I/O/ cells (PICs) 104. It is these PICs 104 that Examiner cites as the plurality of interface groups having a plurality of input multiplexers (e.g., 212).

Applicant respectfully disagrees with Examiner's assertion that Andrews teaches *each* of the PICs has a *plurality* of input multiplexers. As seen in FIG. 2 and the related description, each PIC has *only one* multiplexer, not a *plurality* of input multiplexers. For example, PIC 202 has only one multiplexer 212, PIC 206 has only one multiplexer, PIC 204 has only one multiplexer, and PIC 208 has only one multiplexer. There is no mention or suggestion that any of the PICs has a plurality of input multiplexers. Therefore, Applicants respectfully submit that Examiner has failed to establish that all elements of the invention are disclosed in the prior art.

Furthermore, there is no suggestion or incentive that would motivate one skilled in the art to modify the cited prior art to include a plurality of interface groups, wherein each of the interface groups has a plurality of input multiplexers.

Therefore, Applicants respectfully submit that Claim 1 is non-obvious over Abramovici in view of Andrews, and in further view of Kean and Das.

The same arguments made above with respect to the patentability of Claim 1 are applicable to the patentability of Claims 2 and 3 as well.

Applicants respectfully submit that Claims 1-3 are currently in condition for allowance. Reconsideration and withdrawal of the rejection is respectfully requested.

Claims 4 and 5 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Abramovici, in view of Wells et al. (US 6,651,238), in further view of Andrews, and in even further view of Kean and Das.

The same arguments made above with respect to the patentability of Claim 1 are applicable to the patentability of Claim 4 as well.

Since Claim 5 depends from Claim 4, Applicants respectfully submit that Claim 5 is also patentable as it contains the same limitations as Claim 4.

Therefore, Applicants respectfully submit that Claims 4 and 5 are currently in condition for allowance. Reconsideration and withdrawal of the rejection is respectfully requested.

If the Examiner has any questions regarding this application, the Examiner may telephone the undersigned at 775-586-9500.

Respectfully submitted,
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